普誠科技股份有限公司
Princeton Technology Corp.
Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

DESCRIPTION

PT6313-S is a Vacuum Fluorescent Display (VFD) Controller driven on a 1/4 to 1/8 duty factor. Eight segment output lines, 4 grid output lines, 4 segment/grid output drive lines, one display memory, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip micro computer. Serial data is fed to PT6313-S via a three-line serial interface. It is housed in a 28pins, SOP.

FEATURES

- CMOS Technology
- Low Power Consumption
- Key Scanning (8 x 2 matrix)
- Multiple Display Modes: (8 Segments, 8 Digits to 12 Segments, 4 Digits)
- 8-Step Dimming Circuitry
- Serial Interface for Clock, Data Input, Data Output, Strobe Pins
- No External Resistors Needed for Driver Outputs
- Available in 28pins, SOP

APPLICATION

- Microcomputer Peripheral Devices

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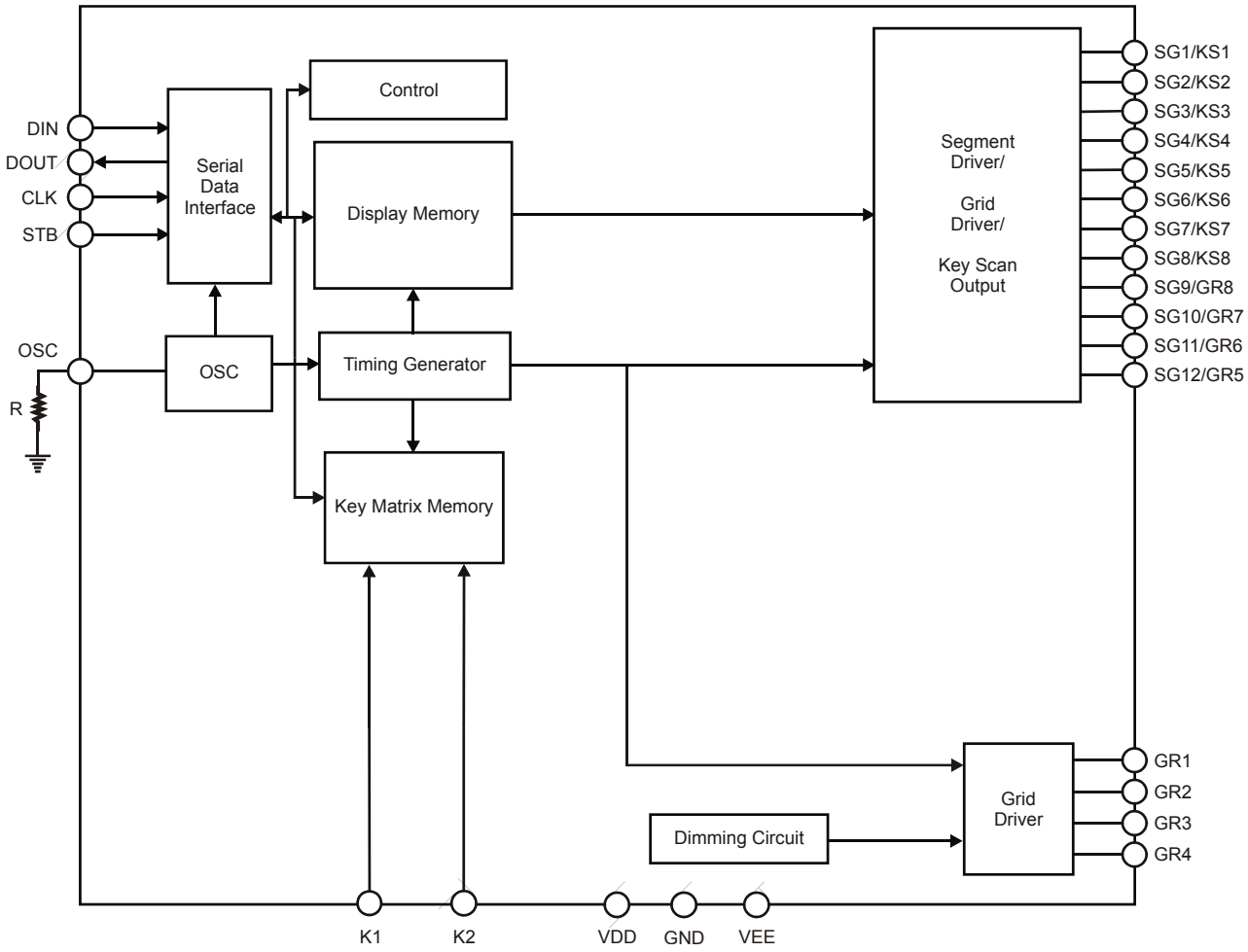
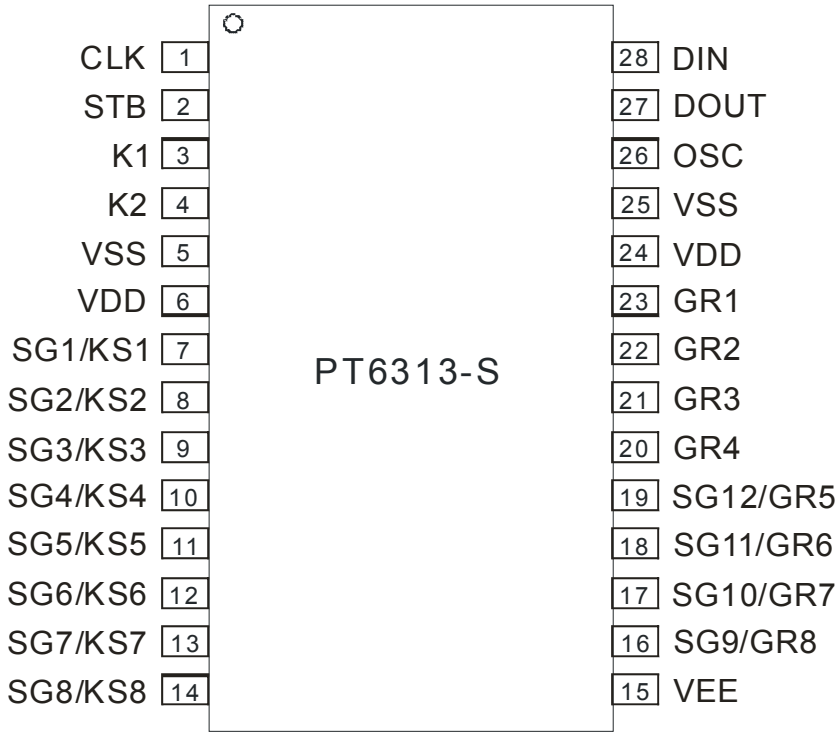
BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
CLK	I	Clock Input Pin This pin reads serial data at the rising edge and outputs data at the falling edge.	1
STB	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command. When this in is "HIGH", CLK is ignored.	2
K1 to K2	I	Key Data Input Pins The data inputted to these pins is latched at the end of the display cycle.	3, 4
VSS	-	Logic Ground Pin	5, 25
VDD	-	Logic Power Supply	6, 24
SG1/KS1 to SG8/KS8	O	High-Voltage Segment Output Pins Also acts as the Key Source.	7 to 14
VEE	-	Pull-Down Level	15
SG9/GR8 to SG12/GR5	O	High-Voltage Segment Output Pins	16 to 19
GR4 to GR1	O	High-Voltage Grid Output Pins	20 to 23
OSC	I	Oscillator Input Pin A resistor is connected to this pin to determine the oscillation frequency.	26
DOUT	O	Data Output Pin (N-Channel, Open-Drain) This pin outputs serial data at the falling edge of the shift clock (starting from the lower bit).	27
DIN	I	Data Input Pin This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit).	28

FUNCTION DESCRIPTION

COMMANDS

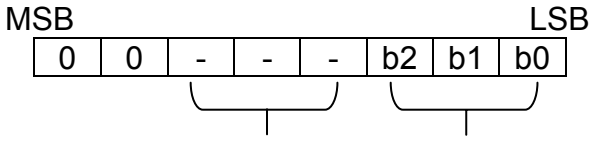
Commands determine the display mode and status of PT6313-S. A command is the first byte (b0 to b7) inputted to PT6313-S via the DIN Pin after STB Pin has changed from “HIGH” to “LOW” State. If for some reason the STB Pin is set to “HIGH” while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

COMMAND 1: DISPLAY MODE SETTING COMMANDS

PT6313-S provides 4 display mode settings as shown in the diagram below: As stated earlier a command is the first one byte (b0 to b7) transmitted to PT6313-S via the DIN Pin when STB is “LOW”. However, for these commands, the bits 4 to 6 (b3 to b5) are ignored, bits 7 & 8 (b6 to b7) are given a value of “0”.

The Display Mode Setting Commands determine the number of segments and grids to be used (1/4 to 1/8 duty, 12 to 8 segments).

When Power is turned “ON”, the 8-digit, 8-segment mode is selected.



Not Relevant

Display Mode Settings:
000: 4 digits, 12 segments
001: 5 digits, 11 segments
010: 6 digits, 10 segments
011: 7 digits, 9 segments
100: 8 digits, 8 segments

Display Mode and RAM Address

Data transmitted from an external device to PT6313-S via the serial interface are stored in the Display RAM and are assigned addresses. The RAM Addresses of PT6313-S are given below in 8 bits unit.

SG1	SG4	SG5	SG8	SG9	SG12	
00HL		00HU		01HL		DIG1
02HL		02HU		03HL		DIG2
04HL		04HU		05HL		DIG3
06HL		06HU		07HL		DIG4
08HL		08HU		09HL		DIG5
0AHL		0AHU		0BHL		DIG6
0CHL		0CHU		0DHL		DIG7
0EHL		0EHU		0FHL		DIG8

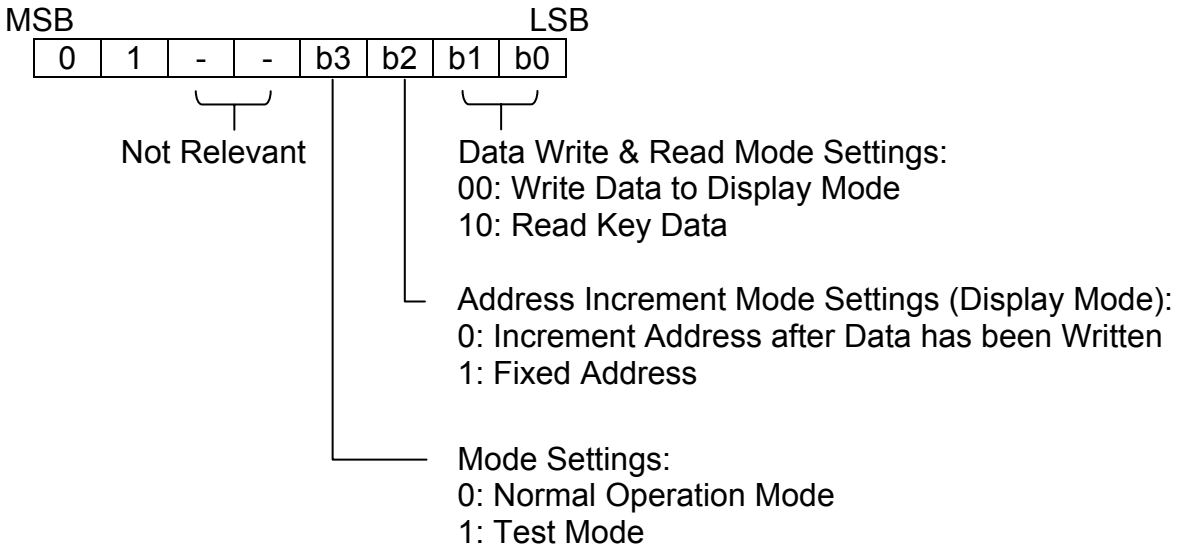
-

b0	b3	b4	b7
xxHL		xxHU	
Lower 4 bits		Higher 4 bits	

COMMAND 2: DATA SETTING COMMANDS

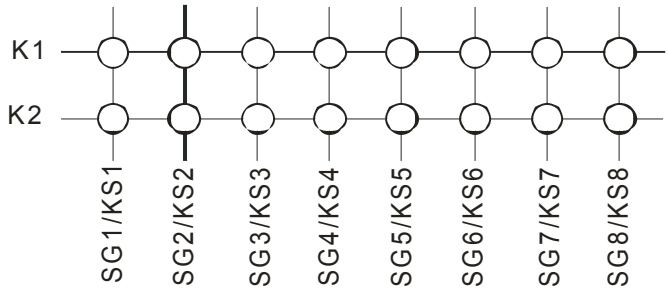
The Data Setting Commands executes the Data Write or Data Read Modes for PT6313-S. The Data Setting Command, the bits 5 and 6 (b4, b5) are ignored, bit 7 (b6) is given the value of “1” while bit 8 (b7) is given the value of “0”. Please refer to the diagram below.

When power is turned ON, the bit 4 to bit 1 (b3 to b0) are given the value of “0”.



PT6313-S Key Matrix & Key Input Data Storage RAM

PT6313-S Key Matrix consists of 8 x 2 array as shown below:



Each data inputted by each key are stored as follows. They are read by a READ Command, starting from the last significant bit. When the most significant bit of the data (SG8, b7) has been read, the least significant bit of the next data (SG1, b0) is read.

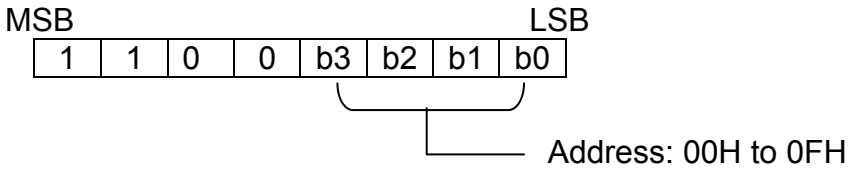
K1……K1	K2……K3	K4……K5	K6……K7
SG1/KS1	SG2/KS2	SG3/KS3	SG4/KS4
SG5/KS5	SG6/KS6	SG7/KS7	SG8/KS8
b0……b1	b2……b3	b4……b5	b6……b7

Reading Sequence

COMMAND 3: ADDRESS SETTING COMMANDS

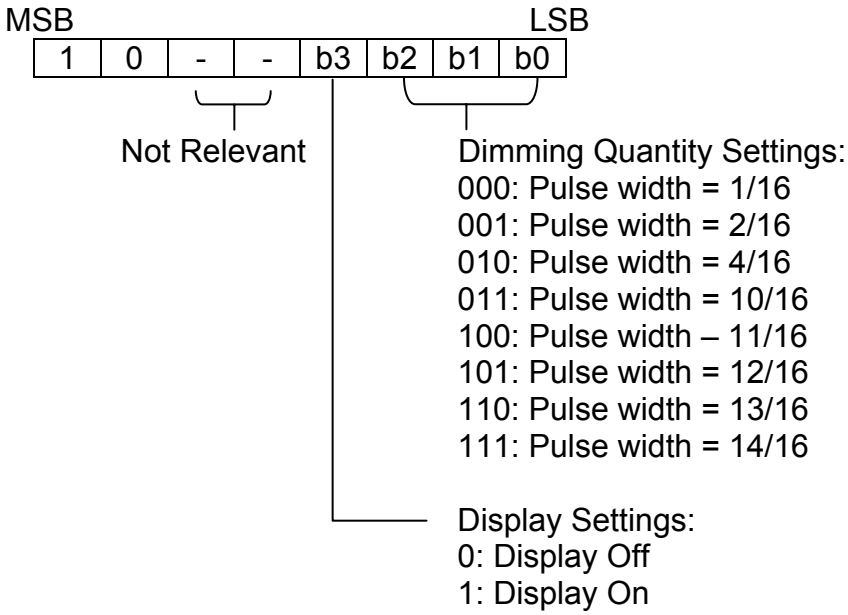
Address Setting Commands are used to set the address of the display memory. The address is considered valid if it has a value of “00H” to “0FH”. If the address is set to 10H or higher, the data is ignored until a valid address is set. When power is turned ON, the address is set at “00H”.

Please refer to the diagram below.



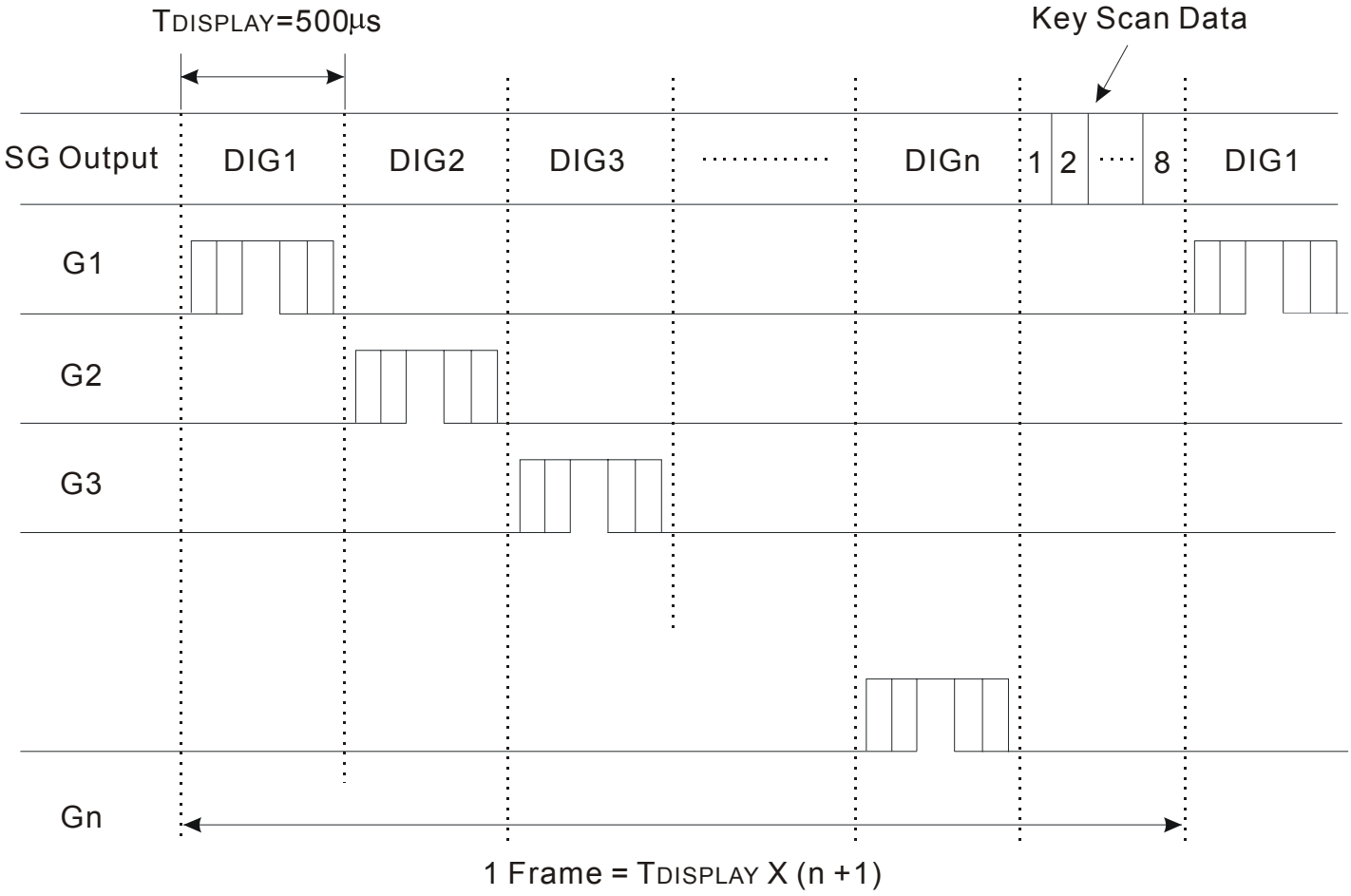
COMMAND 4: DISPLAY CONTROL COMMANDS

The Display Control Commands are used to turn ON or OFF a display. It also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 pulse width is selected and the displayed is turned OFF.



SCANNING AND DISPLAY TIMING

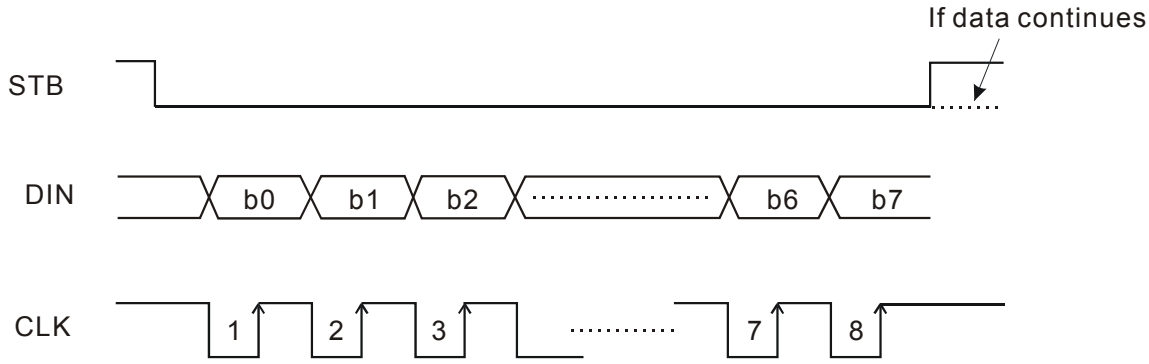
The Key Scanning and display timing diagram is given below. The data of the 8 x 2 matrix is stored in the RAM.



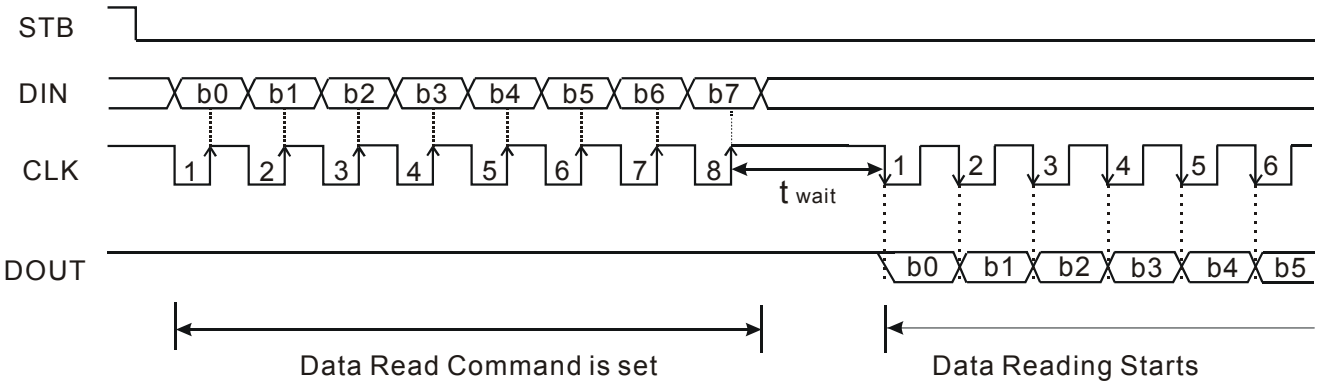
SERIAL COMMUNICATION FORMAT

The following diagram shows the PT6313-S serial communication format. The DOUT Pin is an N-channel, open-drain output pin; therefore, it is highly recommended that an external pull-up resistor (1KΩ to 10KΩ) must be connected to DOUT.

Reception (Data/Command Write)



Transmission (Data Read)

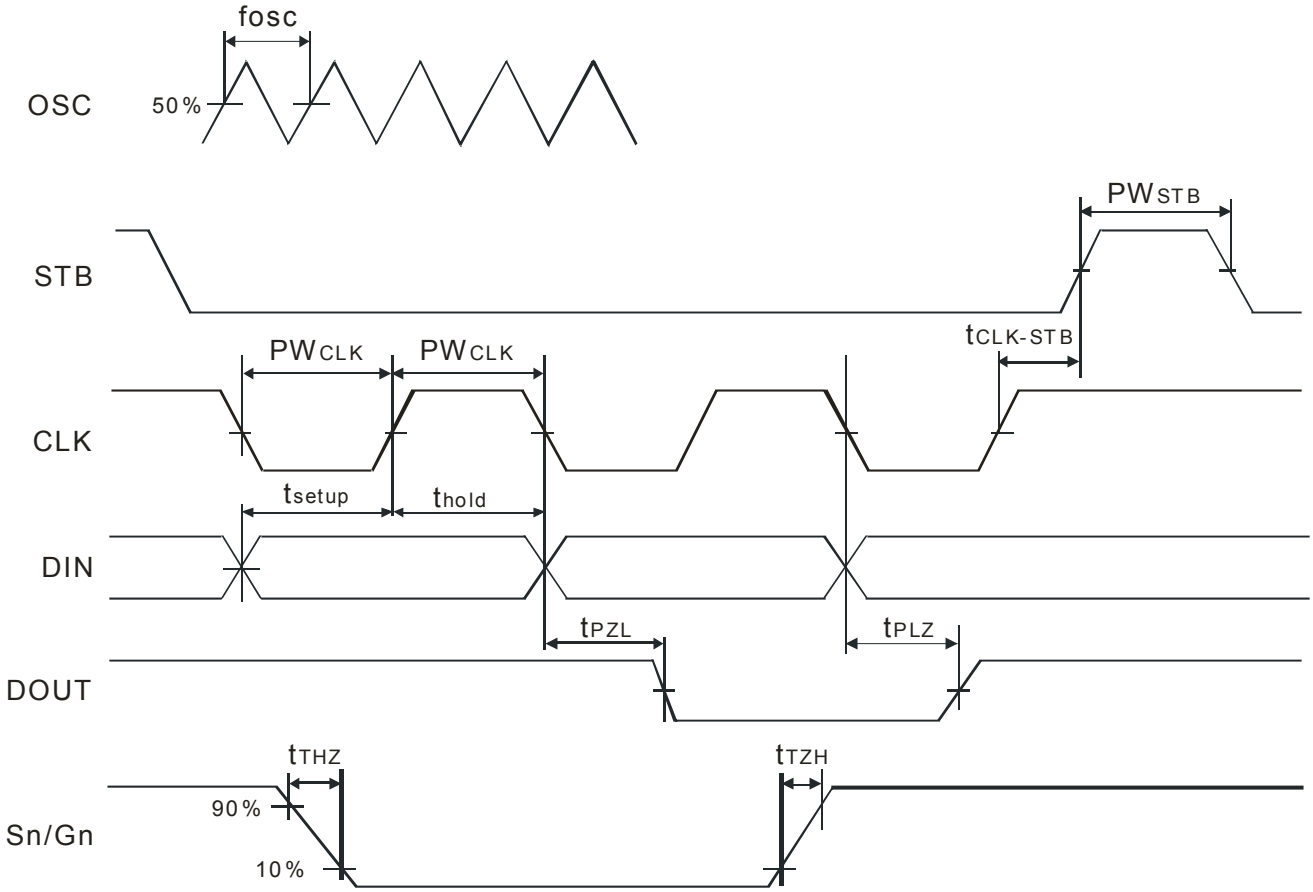


where: twait (waiting time) > 1μs

It must be noted that when the data is read, the waiting time (twait) between the rising of the eighth clock that has set the command and the falling of the first clock that has read the data is greater or equal to 1μs.

SWITCHING CHARACTERISTIC WAVEFORM

PT6313-S Switching Characteristics Waveform is given below.



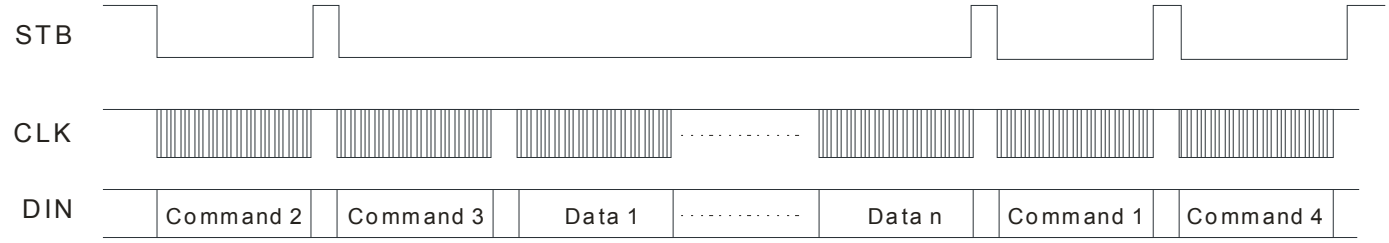
where:

PW CLK (Clock Pulse Width) ≥ 400ns
t setup (Data Setup Time) ≥ 100ns
tCLK-STB (Clock - Strobe Time) ≥ 1μs
tTZH (Grid Rise Time) ≤ 0.5μs (VDD=5V)
tTZH (Grid Rise Time) ≤ 1.0μs (VDD=3.3V)
tTZH (Segment Rise Time) ≤ 2.0μs (VDD=5V)
tTZH (Segment Rise Time) ≤ 3.0μs (VDD=3.3V)
fosc=Oscillation Frequency

PW STB (Strobe Pulse Width) ≥ 1μs
thold (Data Hold Time) ≥ 100ns
tTHZ (Fall Time) ≤ 150μs
t PZL (Propagation Delay Time) ≤ 100ns
tPLZ (Propagation Delay Time) ≤ 400ns

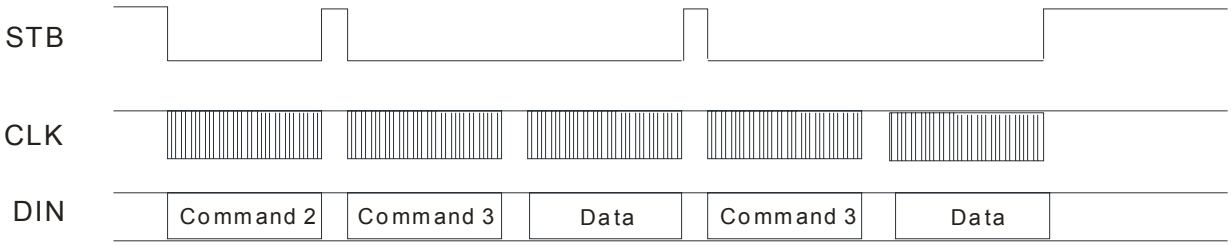
APPLICATIONS

Display memory is updated by incrementing addresses. Please refer to the following diagram.



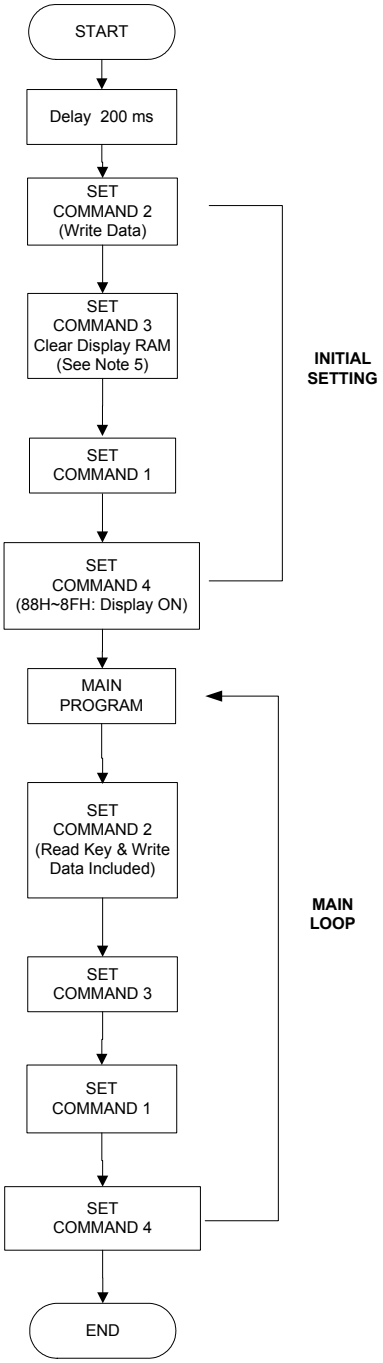
where:
Command 1: Display Mode Setting Command
Command 2: Data Setting Command
Command 3: Address Setting Command
Data 1 to n: Transfer Display Data (16 Bytes max.)
Command 4: Display Control Command

The following diagram shows the waveforms when updating specific addresses.



where:
Command 2: Data Setting Command
Command 3: Address Setting Command
Data: Display Data

RECOMMENDED SOFTWARE FLOWCHART



Note:
1. Command 1: Display Mode Commands
2. Command 2: Data Setting Commands
3. Command 3: Address Setting Commands
4. Command 4: Display Control Commands
5. When IC power is applied for the first time, the contents of the Display RAM are not defined; thus, it is strongly suggested that the contents of the Display RAM must be cleared during the initial setting.

ABSOLUTE MAXIMUM RATINGS

(Unless otherwise stated, Ta=25℃, GND=0V)

Parameter	Symbol	Ratings	Unit
Logic Supply Voltage	VDD	-0.5 to +7	V
Driver Supply Voltage	VEE	VDD +0.5 to VDD -40	V
Logic Input Voltage	VI	-0.5 to VDD +0.5	V
VFD Driver Output Voltage	VO	VEE -0.5 to VDD +0.5	V
VFD Driver Output Current	IOVFD	-40 (Grid) -15 (Segment)	mA
Operating Temperature	Topr	-40 to +85	℃
Storage Temperature	Tstg	-65 to +150	℃

RECOMMENDED OPERATING RANGE

(Unless otherwise stated, Ta=-25℃, GND=0V)

Parameter	Symbol	Ratings			Unit
		Min.	Typ.	Max.	
Logic Supply Voltage	VDD	3.0	5	5.5	V
High-Level Input Voltage	VIH	0.7VDD	-	VDD	V
Low-Level Input Voltage	VIL	0	-	0.3VDD	V
Driver Supply Voltage	VEE	VDD -35	-	0	V

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, VDD=5V, GND=0V, VEE=VDD-35 V, Ta=25℃)

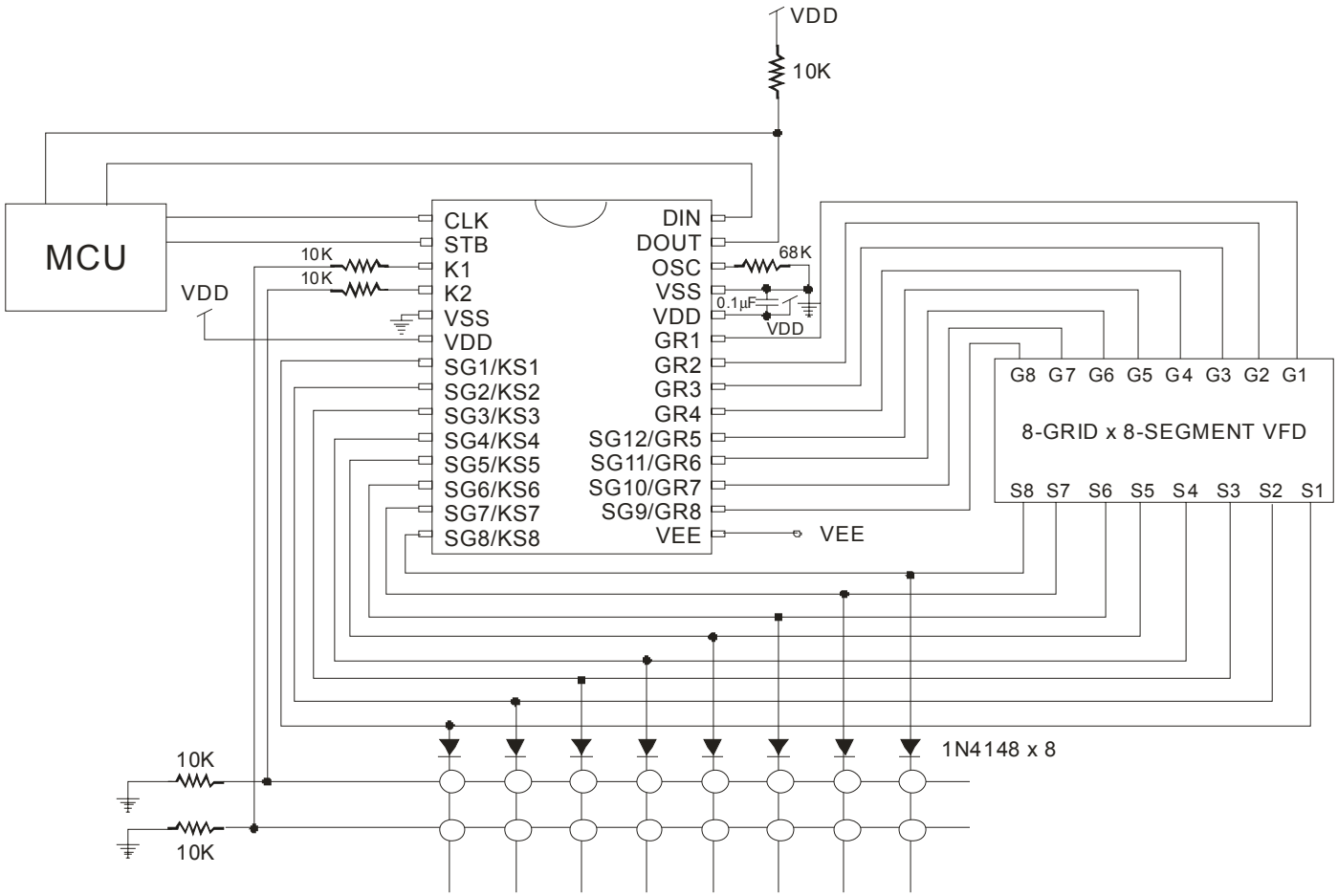
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Low-Level Output Voltage	VOLDOUT	DOUT, IOLDOUT=4mA	-	-	0.4	V
High-Level Output Current	IOHSG	VO=VDD -2V SG1/KS1 to SG8/KS8	-3	-	-	mA
High-Level Output Current	IOHGR	VO=VDD -2V GR1 to GR4, SG9/GR8 to SG12/GR5	-15	-	-	mA
High-Level Input Voltage	VIH	-	0.7VDD	-	VDD	V
Low-Level Input Voltage	VIL	-	-	-	0.3VDD	V
Oscillation Frequency	fosc	R=68KΩ	350	500	650	KHz
Input Current	II	VI=VDD or VSS	-	-	±1	μA
Dynamic Current Consumption	IDDdyn	Under no load Display OFF	-	-	5	mA

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, VDD=3.3V, GND=0V, VEE=VDD-35 V, Ta=25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Low-Level Output Voltage	VOLDOUT	DOUT, IOLDOUT=4mA	-	-	0.4	V
High-Level Output Current	IOHSG	VO=VDD -2V SG1/KS1 to SG8/KS8	-1.5	-	-	mA
High-Level Output Current	IOHGR	VO=VDD -2V GR1 to GR4, SG9/GR8 to SG12/GR5	-6	-	-	mA
High-Level Input Voltage	VIH	-	0.7VDD	-	VDD	V
Low-Level Input Voltage	VIL	-	-	-	0.3VDD	V
Oscillation Frequency	fosc	R=68KΩ	350	500	650	KHz
Input Current	II	VI=VDD or VSS	-	-	±1	μA
Dynamic Current Consumption	IDDdyn	Under no load Display OFF	-	-	3	mA

APPLICATION CIRCUIT



Note: The capacitor (0.1µF) connected between the GND and the VDD pins must be located as close as possible to the PT6313-S chip.

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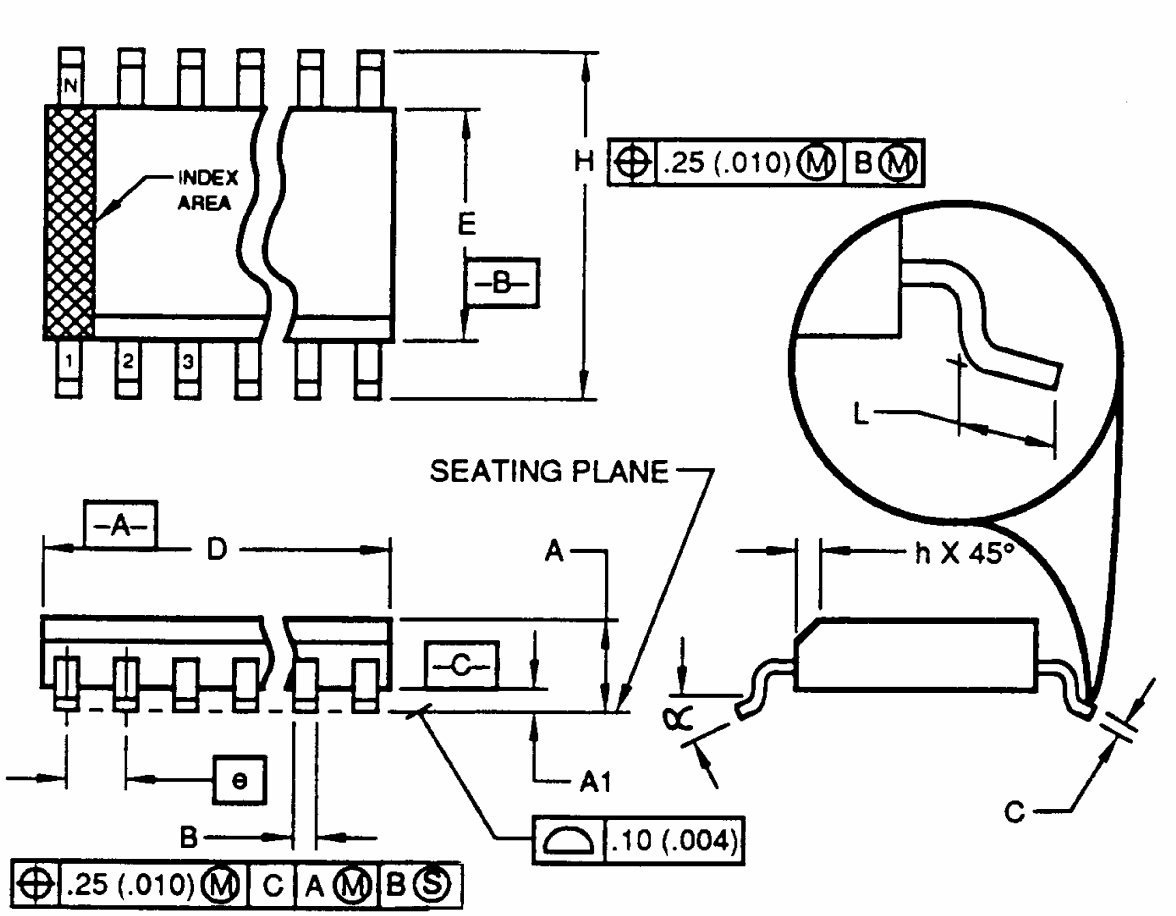
ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6313-S	28pins, SOP, 300mil	PT6313-S
PT6313-S (L)	28pins, SOP, 300mil	PT6313-S

Notes:
1. (L), (C) or (S) = Lead Free.
2. The Lead Free mark is put in front of the date code.

PACKAGE INFORMATION

28 PINS, SOP, 300 MIL



Symbol	Min.	Max
A	2.35	2.65
A1	0.10	0.30
B	0.33	0.51
C	0.23	0.32
D	17.70	18.10
E	7.40	7.60
e	1.27 bsc.	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0^{o}	8^{o}

Notes:
1. Dimensioning and tolerancing per ANSI Y14.5-1982.
2. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.15mm (0.006 in) per side.
3. Dimension E does not include interlead flash or protrusions. Interlead flash and protrusion shall not exceed 0.15mm (0.016in) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. L is the length of terminal for soldering to a substrate.
6. N is the number of terminal positions (N=28).
7. The lead width B as measured 0.36mm (0.014in) or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024 in).
8. Controlling dimension: MILLIMETER
9. Refer to JEDEC MS-013 Variation AE.

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